Model 880770 CPU White Paper

The 880770 CPU is designed to provide faster active to redundant CPU switch over times on the IMACS controller shelf. This capability has been achieved by a major redesign of the existing CPU and Interface (IF) card hardware. The primary design goal is to provide a more stable environment for public safety services and mission-critical networks by significantly reducing or eliminating service interruption during the CPU switch over process. The previous CPU hardware platform (880370) has typical switch over and recovery time of approximately 12 seconds from the time of the switch to when data is recovered. The new 880770 CPU hardware is designed to reduce CPU switch over and recovery time to less than 250 micro seconds; essentially less than two T1 frames.

In order to provide this capability, the IMACS required changes to the Interface (IF) card and CPU card hardware designs, as well as rudimentary software design changes. These changes focused the Interface card's system clocking and the NVRAM storage of the system configuration database. Change requirements can be abbreviated into three major components:

1. Improve IF card robustness by removing all active system controller functions (system clock and system image NVRAM storage) from the IF card and providing a replaceable OAM controller sub-unit half height card to main IF card frame which maintains copper connectivity to the T1/E1 WAN bus.
2. Mirror system controller functions (system clock and system image NVRAM storage) on both active/standby CPU cards facilitating hot standby redundancy.
3. Provide fully serviceable NVRAM and clock interface by using a sub-unit module on the main CPU board that can be replaced on the inactive CPU card.

To accomplish these goals, the 880770 CPU is compatible with only the following new Interface Cards:

- 893270 IMACS,RDNT,I/F,EXT SYNC,8P,NO MODEM
- 893370 IMACS,RDNT,I/F,8P,MODEM
- 893470 IMACS,RDNT,I/F,W/O MODEM

Due to the requirement for a new Interface card design to support fast switch over CPU redundancy, when migrating from 3.x, 5.x, or 6.x CPU based systems both the CPU and IF card hardware must be upgraded as a set. The previously existing IMACS system's configuration will need to be provisioned manually into the new 7.x.y based CPU and IF cards. New 7.x.y based card hardware can be pre-loaded with a system configuration and then inserted into an existing chassis to minimize service interruption.

The 880770 CPU is compliant with the European Union's Reduction of Hazardous Substances (RoHS) directive currently with the lead waiver. The 880770 CPU will support all of the features of the 880370 cards and features in the v6.x.y Host Code versions. Initially, only certain WAN, Server and User cards have been enabled to switch traffic from one CPU to the other in less then 250 micro seconds. These cards are:

SERVER	**DATA**	**VOICE**
IPR*4	SRU	FXS
ADPCM	LD-SRU	FXO
WAN	HSU	E&M
	OHSU	

The 880770 card is designed and supported as a redundant CPU configuration only. Single-processor deployment in the CPU 7.x.y stream is not supported. Should a single-processor arrangement be desired, the customer would deploy a CPU-6 based system.

The 880770 CPU will operate with Host Code versions v7.0.0 and higher. Feature content that is available in Host Code v6.1.2 is supported and carried over to the 7.x.y feature set. Documentation will be revised to present content to the user of currently supported card types for sale by Zhone Technologies. Older and obsolete cards may or may not operate properly in CPU 7.x.y host code release, and will not be supported for the less then 250 micro second processor switch over.

Hardware Details:

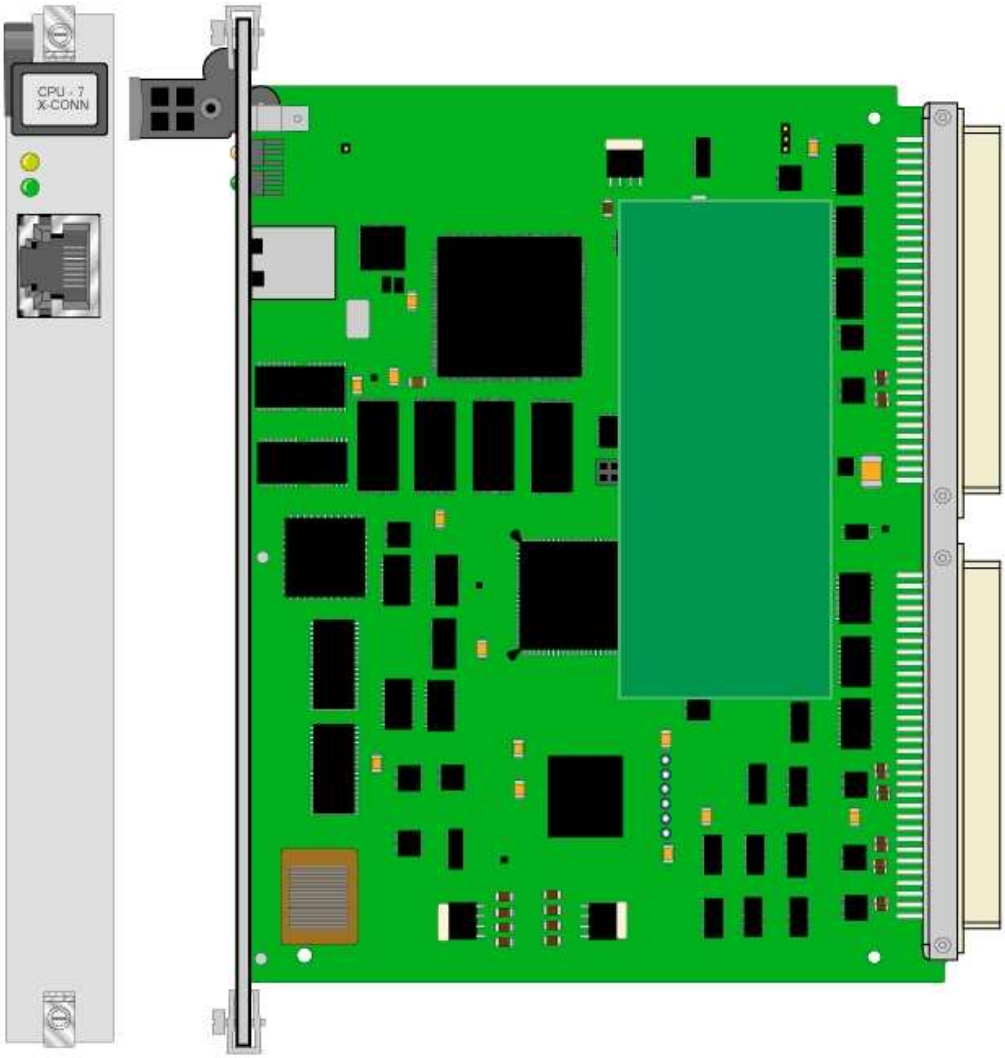


Figure 1: CPU-7 Redundancy card

CPU-7 Features

LED indicators:

- Green for normal operation.
- Yellow for card fault or test mode.

Daughter card

- Contains system clock
- Contains active system configuration in NVRAM
- Clock and NVRAM data constantly synchronizes with the redundant unit to allow for very fast switchovers.

Support of CPU redundancy

- Provides a less-than 250 microsecond active to redundant CPU switchover times.

Hardware dependencies

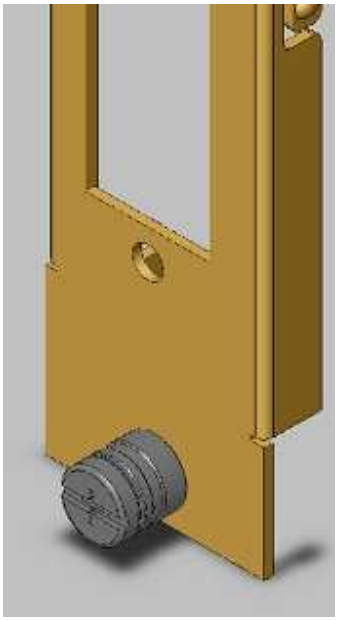
- Must be used with new 893x Interface cards.

Cross connect:

- Same operation as previous IMACS processors.
- 248 timeslots at 64Kbps in each direction, non-blocking.
- Cross connect up to 248 64 Kbps timeslots on 8 T1 or E1 links in a non-blocking configuration

Upgrading to the new 880770 CPU

- Upgrade to the 880770 is not supported. The 880770 is intended for new start-up systems using the new Interface and CPU boards.



The new 880770 and 893x series of Interface cards comes with an improved fastener system. This system allows for removing or tightening the fastener via thumb, Phillips or a slotted screwdriver

Figure 2: Fasteners

The new 893270, 893370 and 893470 Interface cards – carry forward all the existing capabilities and features of the 892260, 892360 and 892460 traditional Interface card designs. As an improvement to the survivability of the IMACS shelf, the boards have been split into two main sections as shown in the following illustration.

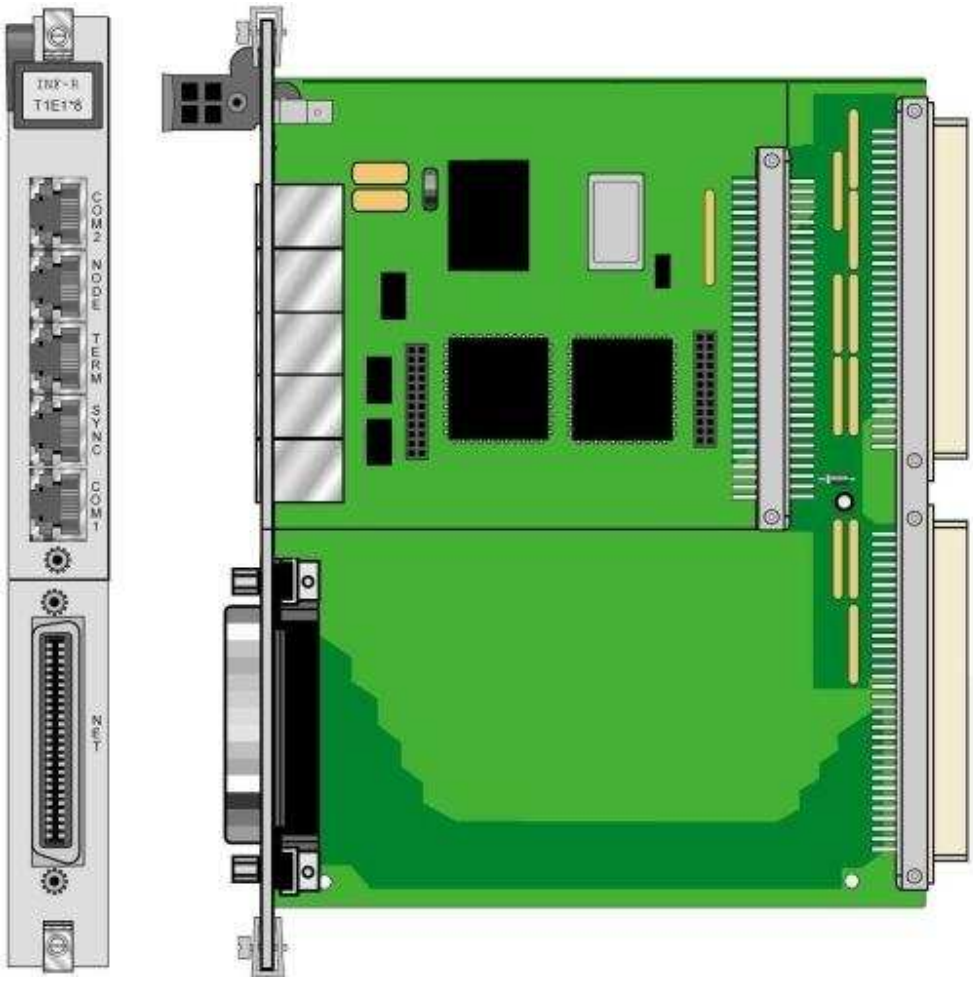


Figure 3: PRM-8932 Ext Sync Interface Redundancy card

The lower portion of the card provides for a totally passive path from the input point on the faceplate to the backplane of the IMACS shelf for the WAN E1 or T1 signals. This provides for non-interrupted ability to service the Interface card, as all active components traditionally carried by the interface card (modem, terminal driver, external sync interfaces, etc.) have been moved to a separate board sub-unit on the main Interface card. This board sub-unit can be replaced in the field without WAN service interruption should any of these components fail. New with the introduction of the 893x series of Interface cards is an OOS alarm should this service on the board sub-unit become necessary.

Also introduced into the Host code v7.x.y is enhanced security features first introduced in the IMACS 200 platform. These new security features include the addition of a user name in conjunction with a password, whereas the original IMACS system used a password security only. This new capability is illustrated below.

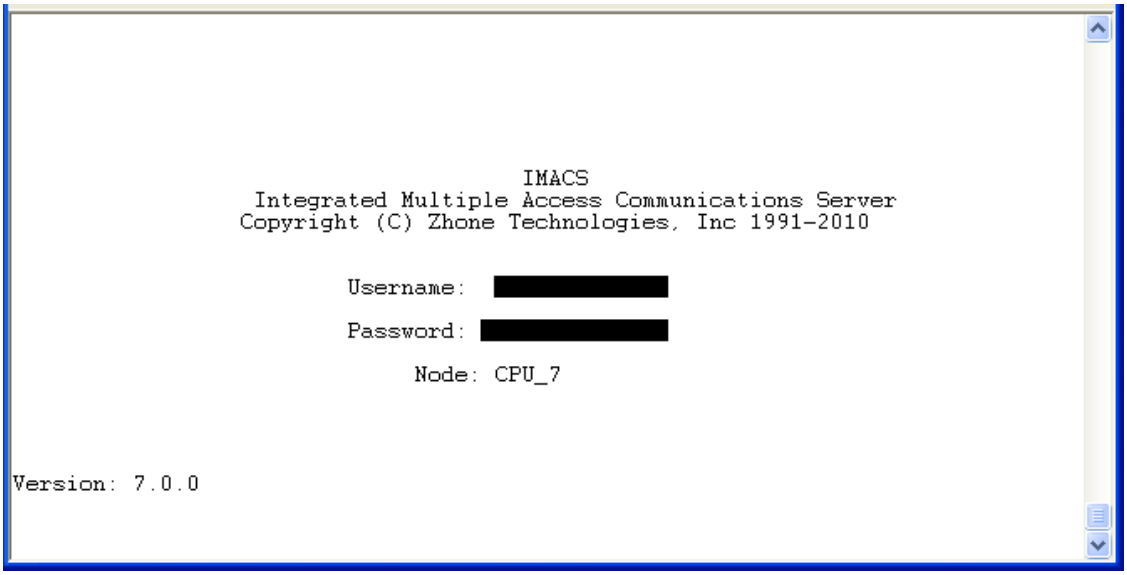


Figure 4: New Login Methodology

The username and password, along with assignable access privileges are flexible and can be set up by the system administrator. Up to 256 specific username login/password combinations can be assigned. In addition, the system now logs time of day changes, log clearing events, as well as user log in and log out events.

Additional features targeted only for the CPU-7 host code stream are:

Configuration change log
TACACS+
Encryption
Network NTP timing
Multiple mapping tables
Redundant NVRAM copies kept on-board

Following is the CPU-7 backplane switch methodology diagram.

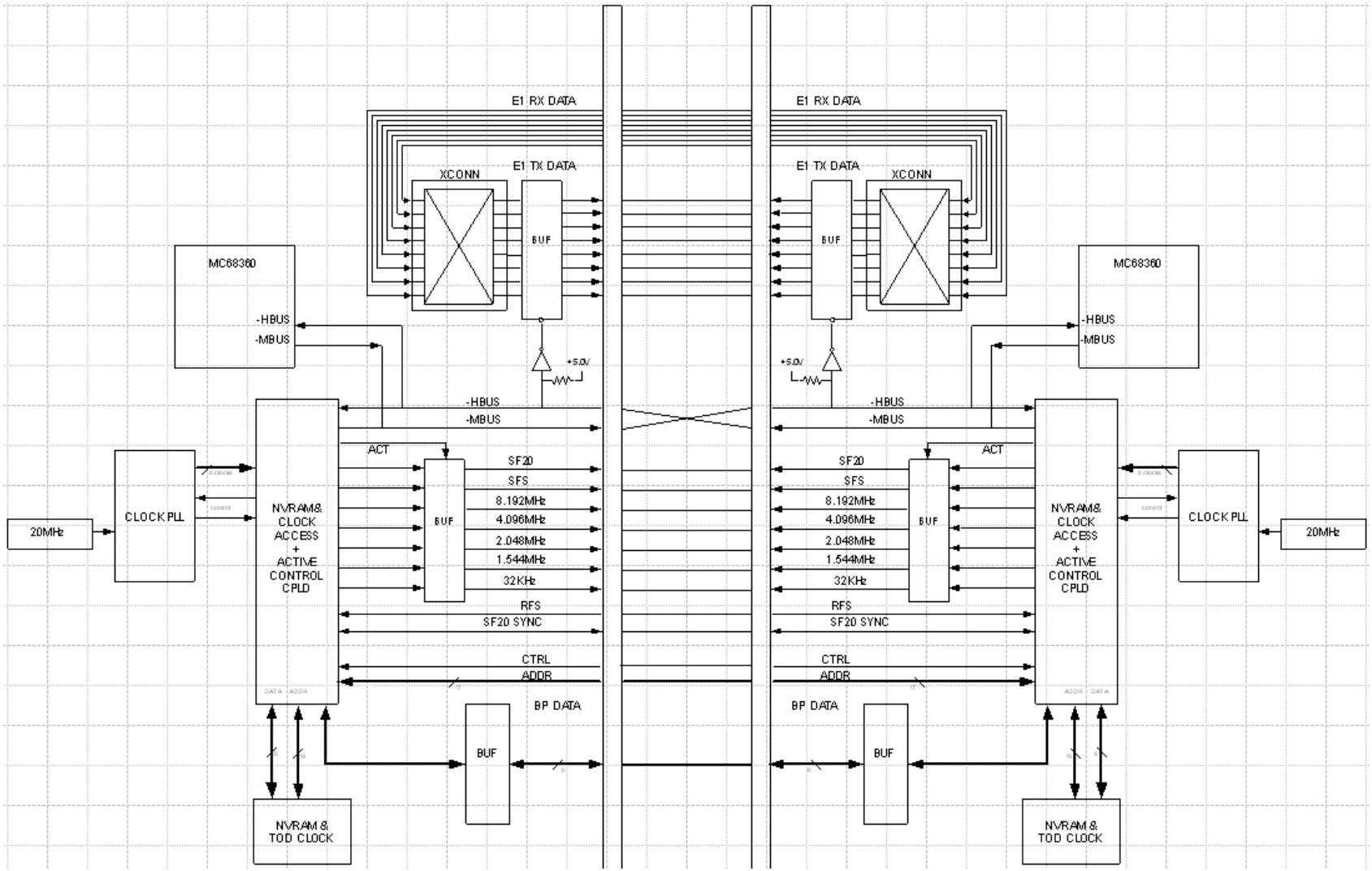


Figure 5: CPU-7 Switch Block Diagram